DATA SHEET

SUNPLUS

SPCP02A

Keyboard Controller

AUG. 05, 2003

Version 1.1

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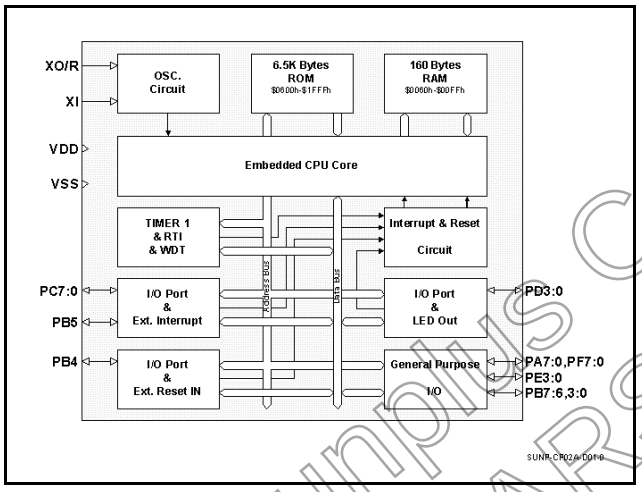
KEYBOARD CONTROLLER

1. GENERAL DESCRIPTION

SPCP02A, a 44-pad micro-controller, contains an 8-bit timer, a watchdog timer and 40 general-purpose I/Os that can easily be applied for keyboard applications. Inside the chip, the 8-bit CPU is able to work at the maximum operating frequency of 6MHz. The embedded ROM size is 6.5K bytes, and the embedded SRAM is 160 bytes. In addition, it supports 40/48-pin packages or 44-pad COB solution.

2. BLOCK DIAGRAM



3. FEATURES

- Built-in 8-bit Sunplus CPU core and up to 6MHz clock operation.
- 40 or 36 general-purpose I/Os that are belong to six groups of I/O ports. Some of them are combined with the options of pull-up/down resistors, or totem pole/open drain outputs
- Four I/O ports can be utilized for LED outputs.
- Two external interrupt groups -- one comes from individual I/O (PB5); the other is a group input, PC port. They can be enabled by mask option.
- External reset input option on PB4.
- One 8-bit timer with real time interrupt control.
- A watchdog timer for program control.
- 6.5K bytes of ROM with 160 bytes of RAM.
- R-Oscillation or crystal input options for system clock.
- Stop control setting for power saving mode.
- Operating voltage range: 2.4V - 5.5V.

4. SIGNAL DESCRIPTIONS

Mnemonic	40 PIN PKG	48 PIN PKG	44 PAD COB	Description
VSS	1	42	1	*System Ground.*
PD3	2	43	2	*GPIO Port D3 Output (LED Output 3).* This I/O channel can be LED high current driven output or general I/O. Use internal setting to configure it.
PE0:1	3:4	44:45	3:4	*GPIO Port E0:1.* General-purpose input/output or PS/2 interface by programming configuration.
PE2:3		46:47	5:6	*GPIO Port E2:3.* General-purpose input/outputs or PS/2 interface by programming configuration.
PB0:3	5:8	48,1:3	7:10	*GPIO Port B0:3.* General-purpose input/outputs by programming configuration.
PB4:5	9:10	4:5	11:12	*GPIO Port B4:5.* General-purpose inputs/output by programming configuration. In addition, PB4 can be used as the Main RESET input. PB5 can be used as the external Main IRQ input.
PB6:7		6:7	13:14	*GPIO Port B6:7.* General-purpose input/outputs by programming configuration.
PA0:7	11:18	8:15	15:22	*GPIO Port A0:7.* General-purpose input/outputs by programming configuration.
PF0:7	19:26	16:23	23:30	*GPIO Port F0:7.* General-purpose input/outputs by programming configuration.
PC0:7	27:34	28:35	31:38	*GPIO Port C0:7.* General-purpose inputs/outputs by programming configuration. In addition, these pins can be used as the external interrupt inputs.
PD0:2	35:37	36:38	39:41	*GPIO Port D0:2 Output (LED Output 0:2).* These I/O channels can be LED high current driven outputs or general I/Os by programming configuration.
VDD	38	39	42	*System Power Supply.*
XO/R	39	40	43	*Crystal In or Resistor In Input.* An external resistive pull-up connects with internal OSC circuitry for generating the internal clock and the related time base in R-Oscillation mode. It will be connected with external crystal for a crystal oscillation circuitry in crystal mode.
XI	40	41	44	*Crystal Output or External Clock Input.* External clock input connects with internal clock circuitry to generate the internal clock and related time base in external clock mode. It will be connected with external crystal for a crystal oscillation circuitry in crystal mode.

Note: for package type LQFP 48 the followings are NC pin: 24, 25, 26, 27

4.1. Ordering Information

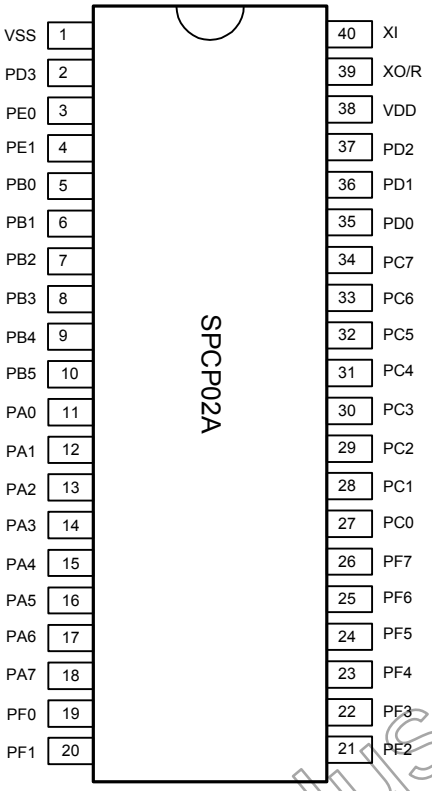
Product Number	Package Type
SPCP02A-NnnV-C	Chip form
SPCP02A-NnnV-PD12	Package form - PDIP 40
SPCP02A-NnnV-PL23	Package form - LQFP 48

Note1: Code number is assigned for customer.

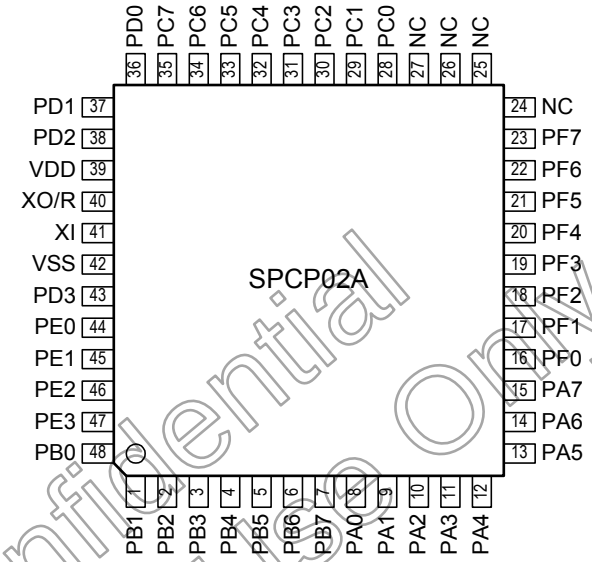
Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

4.2. PIN Assignment

4.2.1. PDIP 40 PIN



4.2.2. LQFP 48 PIN



5. FUNCTIONAL DESCRIPTIONS

5.1. CPU

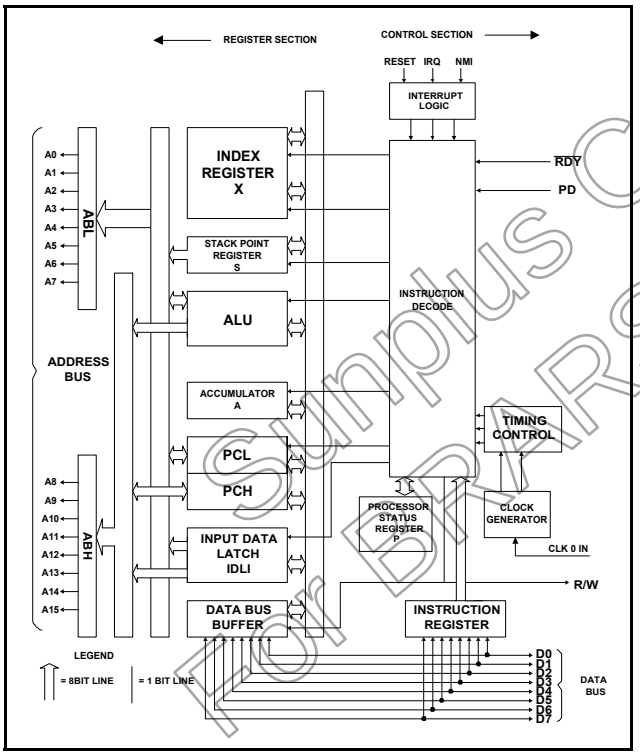
The microprocessor of SPCP02A is a SUNPLUS high performance processor equipped with Accumulator, Program Counter, X Register, Stack Pointer and Processor Status Register (The same as 6502 instruction structure). SPCP02A is a fully static CMOS design. The oscillation frequency can be run up to 6.0MHz depends on the application needs.

5.1.1. Processor status register

Bit	7	6	5	4	3	2	1	0
Flag	N	V	-	B	-	I	Z	C

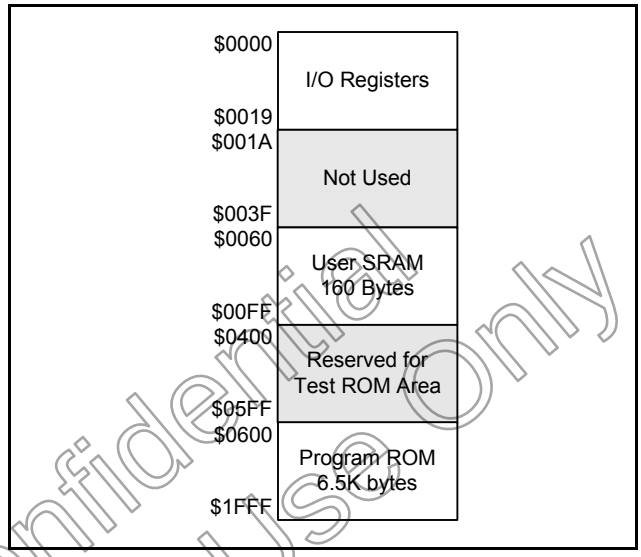
N: Negative, V: Overflow, B: Brk command, I: IRQ disable, Z: Zero, C: Carry

5.1.2. Block diagram of SUNPLUS CPU



5.2. Memory

5.2.1. Memory map



5.2.2. RAM

Total of 160 bytes of RAM (including the stack) is available from $0060 to $00FF. The stack begins at address $00FF and proceeds down to $0060.

5.2.3. ROM

The 7168 bytes of ROM on chip include 6656 bytes of user ROM (located from $0600 through $1FFF) and 512 bytes of internal test ROM (located from $0400 through $05FF). User's program can only be allocated from $0600 through $1FFF (6.5K).

5.2.4. NMI, reset, IRQ vectors

The address of NMI (not provided in this chip), RESET and IRQ are located from $1FFA to $1FFF. The interrupt vectors must be specified in the program as follows:

```
ORG     $1FFA           ; define SPCP02A chip
                        ; interrupt vector.
DW      NMI_ROUTINE
DW      RESET
DW      INT_ROUTINE
```

When using emulation board with EPROM (for 27C256), the address of $7FFA must be defined as follows:

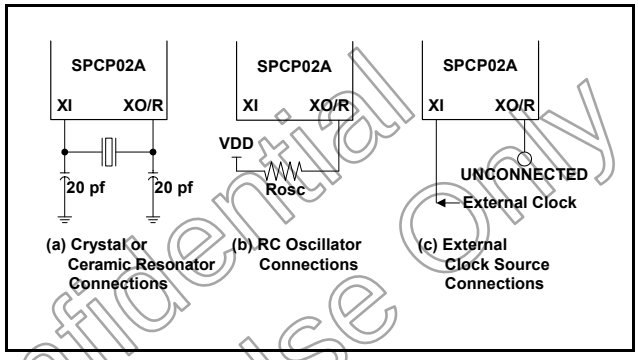
```
ORG     $7FFA           ; interrupt vector for
                        ; EPROM with
DW      NMI_ROUTINE     ; Emulation Board.
DW      RESET
DW      INT_ROUTINE
```

When using emulation board with Sunplus ICE, users fill the **ORG** address of $0FFFA as follows:

```
ORG     $0FFFA          ; interrupt vector for
                        ; SUNPLUS ICE.
DW      NMI_ROUTINE
DW      RESET
DW      INT_ROUTINE
```

5.3. Oscillator

The SPCP02A supports AT-cut parallel resonant oscillated Crystal /Resonator, RC oscillator, or external clock sources by mask option (select one from three types). The design of application circuit should follow the vendor's specifications and recommendations. The diagram listed below represents typical X'TAL/ROSC circuits for most applications:



The definitions of mask options for oscillation are:

Option	Relation	Description
clkext	XI, XO	*External Clock Input Option.* This option is combined with the option oscm to select the oscillation mode. The oscillation mode is described below.
oscm	XI, XO	*Oscillation Mode Option.* The oscillation mode is described below.

Mode	Description
External Clock Input Mode	The crystal/resonator buffer is tri-state. External clock input can be connected to XI to generate clock.
Crystal/Resonator Oscillation Mode	A crystal/resonator circuitry is connected to XI and XO to generate clock.
External ROSC Mode	A built-in R-OSC circuitry with an external pull-up resistor placed on XI is enabled to generate clock. The external pull-up resistor determines the operating frequency.

5.4. Control Register Summary

The function blocks have two kinds of control input. One is mask option and the other is programmable register. Mask options are used as permanent assignment. They are configured with the program code at the same time. Once the mask options are written to SPCP02A, they are unchangeable as the program code. The mask options are described in later section. Programmable registers control the function blocks by programming. The program can access the registers to achieve specific functions. The registers are summarized as follows. All function registers will be set to "0" (except *rt1* and *rt0* in ***TCS1***) when a reset signal is given. The bits *rt1* and *rt0* will be set to "1" when a reset signal occurred.

Abbr.	Register	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Enable
Addr.	R/W Control	Default Value								
PA	Port A Data	a7:0								
$0000	a a a a a a a a	0	0	0	0	0	0	0	0	
PB	Port B Data	b7:0								
$0001	a a a a a a a a	0	0	0	0	0	0	0	0	
DPA	Port A Data Direction	dpa7:0								0=IN
$0002	w w w w w w w w	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	1=OUT
DPB	Port B Data Direction	dpb7:0								0=IN
$0003	w w w w w w w w	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	1=OUT
TCS1	Timer Ctl. & Status 1	tof1	rtif	tofe1	rtie	tofr1	rtifr	rt1	rt0	
$0004	r r a a w w a a	0	0	0	0	(0)	(0)	1	1	1=SET
TCR1	Timer Counter Reg. 1	tm1r7:0								
$0005	r r r r r r r r	0	0	0	0	0	0	0	0	
IRQS	IRQ Control & Status		irqr	irqf2	irqe2	irqf			irqe	
$0006	- w r a r - - a	-	(0)	0	0	0	-	-	0	
CPWD	CMP & WDT Status								wdt	
$0007	- - - - - - - w	-	-	-	-	-	-	-	0	1=CLR
SNW	Stop & Wait				stop					
$0008	- - - w - - - -	-	-	-	(0)	-	-	-	-	1=SET
RPA	Port A Pull-up Control	rpa7:0								0=Enable
$0009	w w w w w w w w	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	1=Disable
RPB	Port B Pull-up Control	rpb7:0								0=Enable
$000A	w w w w w w w w	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	1=Disable
RPC	Port C Pull-up Control	rpc7:0								0=Enable
$000B	w w w w w w w w	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	1=Disable
PC	Port C Data	c7:0								
$000C	a a a a a a a a	0	0	0	0	0	0	0	0	
DPC	Port C Data Direction	dpc7:0								0=IN
$000D	w w w w w w w w	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	1=OUT
DPD	Port D Data Direction	iadr	oper	ssr1	ssr0	dpd3	dpd2	dpd1	dpd0	0=IN
$0011	r r r r w w w w	0	0	0	0	(0)	(0)	(0)	(0)	1=OUT
PD	Port D Data			ssr1	ssr0	d3	d2	d1	d0	
$0012	- - w w a a a a	-	-	(0)	(0)	0	0	0	0	
RPD	Port D Pull-up Control					rpd3	rpd2	rpd1	rpd0	0=Enable
$0013	- - - - w w w w	-	-	-	-	(0)	(0)	(0)	(0)	1=Disable
DPE	Port E Data Direction					dpe3	dpe2	dpe1	dpe0	0=IN
$0014	- - - - w w w w	-	-	-	-	(0)	(0)	(0)	(0)	1=OUT

Abbr.	Register	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Enable
Addr.	R/W Control	Default Value								
PE	Port E Data					e3	e2	e1	e0	
$0015	- - - - a a a a	-	-	-	-	0	0	0	0	
RPE	Port E Pull-up/down Ctl.					rpe3	rpe2	rpe1	rpe0	0=Enable
$0016	- - - - w w w w	-	-	-	-	(0)	(0)	(0)	(0)	1=Disable
DPF	Port F Data Direction	dpf7:0								0=IN
$0017	w w w w w w w w	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	1=OUT
PF	Port F Data	f7:0								
$0018	a a a a a a a a	0	0	0	0	0	0	0	0	
RPF	Port F Pull-up Control	rpf7:0								0=Enable
$0019	w w w w w w w w	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	1=Disable

The value in parentheses () is the power-on default value. The gray blocks are reserved.

5.5. Port A Group

The I/O port A has eight programmable I/Os that are controlled by data register (PA), direction control register (DPA), and pull-up resistance control register (RPA). DPA controls the pad I/O attribute. Setting the bit(s) to "1" will enforce the corresponding pad(s) to output mode. It is a write-only register. PA stores the data contents for output. Reading PA will get the stored data when corresponding bit of DPA is set as output mode, or will get the pad status if it is in input mode.

There is a built-in pull-up resistor on each I/O pin. These pull-up resistors can be controlled by user's program through RPA. When the corresponding control bit (rpa_n,) is enabled, the resistor will be activated in input mode. Each I/O channel has Schmitt-Trigger input buffer for input mode. PA7:0 are open-drain outputs in output mode. Setting the direction bit (dpa_n) to "1" with the corresponding data bit (a_n,) to "0" will activate the pad as low. Once the data bit is changed to "1", the I/O pad will become tri-state.

The corresponding pads are assigned for SPCP02A as follows (VDD = 5.0V)

PIN	Rp		IN	OUT	Special Function
PA7	100K	Pull-up @ rpa7	Schmitt-Trigger	-/4mA	-
PA6	100K	Pull-up @ rpa6	Schmitt-Trigger	-/4mA	-
PA5	100K	Pull-up @ rpa5	Schmitt-Trigger	-/4mA	-
PA4	100K	Pull-up @ rpa4	Schmitt-Trigger	-/4mA	-
PA3	100K	Pull-up @ rpa3	Schmitt-Trigger	-/4mA	-
PA2	100K	Pull-up @ rpa2	Schmitt-Trigger	-/4mA	-
PA1	100K	Pull-up @ rpa1	Schmitt-Trigger	-/4mA	-
PA0	100K	Pull-up @ rpa0	Schmitt-Trigger	-/4mA	-

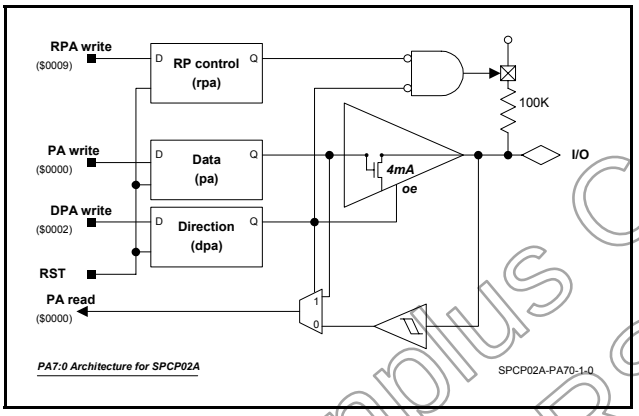
The definitions of registers PA, DPA, and RPA are showed below:

PA	Port A Data Register			$0000
Name	Bit	RW	Dft	Functional Description
a7:0	7:0	A	0h	*Port A Data*. When Port A is programmed as output, the output data on Port A pins are determined by PA data register. When Port A is programmed as input, any "read" command on Port A will reflect the logic status of those I/O pins. PA data register will be set to "0" when RESET occurred.

DPA	Port A Data Direction Register			$0002
Name	**Bit**	**RW**	**Dft**	**Functional Description**
dpa7:0	7:0	W	0h	*Port A Data Direction*. Port A can be programmed as inputs or outputs by DPA register. When **dpa**n="1", the corresponding pins are programmed as outputs. When **dpa**n="0", the corresponding pins are programmed as inputs. The DPA will be set to "0"(input) when RESET occurred.

RPA	Port A Pull-up Control Register			$0009
Name	**Bit**	**RW**	**Dft**	**Functional Description**
rpa7:0	7:0	W	0h	*Port A Pull-up Disable*. When the bit is "0" the built in pull-up resistor of the corresponding pin in input mode will be enabled. When it is "1", the pull-up resistor will be disabled. The pull-up resistors are invalid during output mode. The RPA will be set to "0"(enable mode) by RESET.

The I/O structure of Port A is shown below:



PA7:0 Architecture for SPCP02A

5.6. Port B Group

The I/O Port B has 8 programmable I/Os that are controlled by data register (PB), direction control register (DPB), and pull-up resistance control register (RPB). DPB controls the pad I/O attribute. Setting the bit(s) to "1" will enforce the corresponding pad(s) to output mode. It is a write-only register. PB is able to store the data contents for output. Reading PB will get the stored data when corresponding bit of DPB is set as output mode, or will get the pad status if it is in input mode.

There is a built-in pull-up resistor on each I/O channel. These pull-up resistors can be controlled by user's program through RPB. When the corresponding control bit, (rpb_n,) is enabled, the resistor will be activated in input mode. In case of PB5 interrupt input is enabled by mask option, the pull-up resistor on PB5 is controlled by the mask option of interrupt polarity. Setting rising-edge trigger interrupt on PB5 will disable the pull-up resistor on PB5. If it is configured as falling-edge trigger interrupt input, the resistor on PB5 can be controlled by the bit rpb5 of register RPB.

Each I/O pin has Schmitt-Trigger input buffer for input mode. PB3:0 are open-drain outputs in output mode. Setting the direction bit (dpb_n,) to "1" with the corresponding data bit, (b_n,) to "0" will activate the pad as low. Once the data bit is changed to "1", the I/O pad will become tri-state. PB7:4 can be selected as open-drain outputs or totem-pole outputs by mask options. Once the outputs of PB7:4 are set as totem-pole outputs, the only difference to the open-drain outputs is setting dpb_n to "1" and pb_n, to "1". In this case, the I/O pin will output high.

PB5 can be external interrupt input with falling-edge trigger by enabling the mask option. More details are described in ***Interrupt Chapter***. PB4 can be used as external active-low reset input through mask option.

In 40 pin package, PB7:6 are not present. The values of the correlated data bits or control bits should be kept as the reset default.

The corresponding pads are assigned for SPCP02A as follows (VDD = 5.0V):

PIN	Rp		IN	OUT	Special Function
PB7	100K	Pull-up @ rpb7	Schmitt-Trigger	(4)/4mA	-
PB6	100K	Pull-up @ rpb6	Schmitt-Trigger	(4)/4mA	-
PB5	100K	Pull-up @ rpb5	Schmitt-Trigger	(4)/4mA	IRQ0 interrupt input
PB4	100K	Pull-up @ rpb4	Schmitt-Trigger	(4)/4mA	External nRESET input
PB3	100K	Pull-up @ rpb3	Schmitt-Trigger	-/4mA	-
PB2	100K	Pull-up @ rpb2	Schmitt-Trigger	-/4mA	-
PB1	100K	Pull-up @ rpb1	Schmitt-Trigger	-/4mA	-
PB0	100K	Pull-up @ rpb0	Schmitt-Trigger	-/4mA	-

The definitions of mask options for Port B are:

Option	Relation	Description
aipb5	PB5	*Alternative Input Option on PB5 for IRQ0.* Enable or Disable.
ippb5	PB5	*Polarity Control Option on PB5 for IRQ0.* Low active or falling edge trigger, or High active or rising edge trigger.
aipb4	PB4	*Alternative Input Option on PB5 for IRQ0.* Enable or Disable..
odpb7:4	PB7:4	*Open-Drain Output Option on PB7:4.* Open-drain output or Totem-pole output.

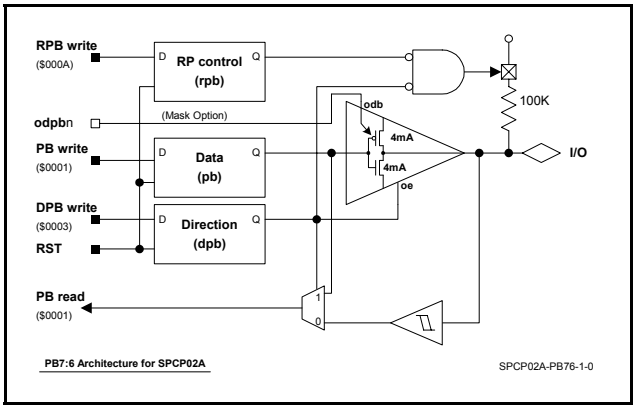
The definitions of registers PB, DPB, and RPB are showed below:

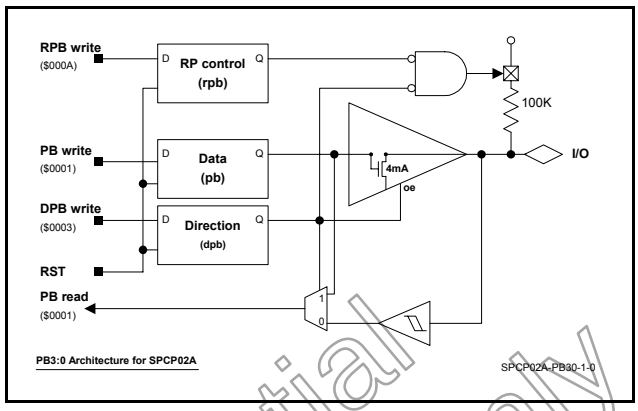
PB	Port B Data Register				$0001
Name	Bit	RW	Dft	Functional Description	
b7:0	7:0	A	0	*Port B Data*. When Port B is programmed as output, the output data on Port B pin are determined by PB data register. When Port B is programmed as input any “read” command on Port B Data Register will reflect the logic status of those I/O pins. PB data register will be set to “0” when RESET occurred.	

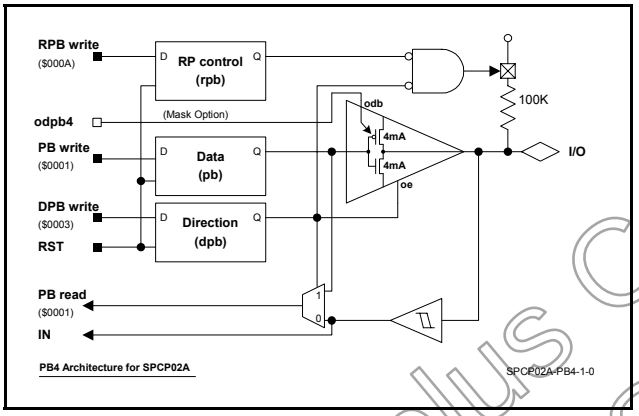
DPB	Port B Data Direction Register				$0003
Name	Bit	RW	Dft	Functional Description	
dpb7:0	7:0	W	0	*Port B Data Direction*. Port B can be programmed as inputs or outputs by DPB register. When **dpb**n=”1”, the corresponding pins are programmed as outputs. When **dpb**n=”0”, the corresponding pins are programmed as inputs. The DPB will be set to “0”(input) when RESET occurred.	

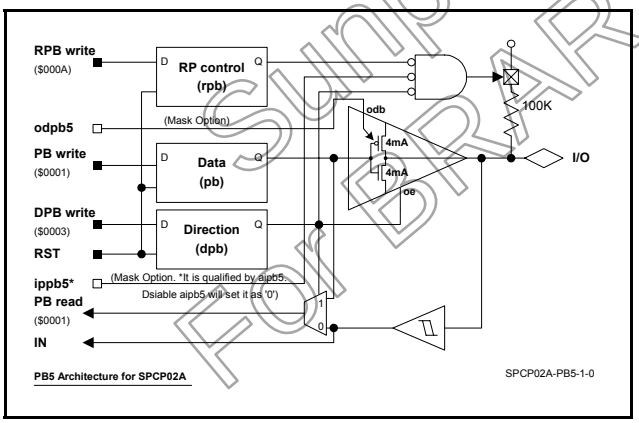
RPB	Port B Pull-up Control Register				$000A
Name	Bit	RW	Dft	Functional Description	
rpb7:0	7:0	W	0h	*Port B Pull-up Disable*. When the bit is “0”, the built in pull-up resistor of the corresponding pin in input mode will be enabled. When it is “1”, the pull-up resistor will be disabled. The pull-up resistors are invalid during output mode. The RPB will be set to “0”(enable mode) by RESET.	

The I/O structures of Port B are shown below:









5.7. Port C Group

The I/O Port C has 8 programmable I/Os that are controlled by data register (PC), direction control register (DPC), and pull-up resistance control register (RPC). DPC controls the pad I/O attribute. Setting the bit(s) to "1" will enforce the corresponding pad(s) to output mode. It is a write-only register. PC stores the data contents for output. Reading PC will get the stored data when corresponding bit of DPC is set as output mode, or will get the pad status if it is in input mode.

There is a built-in pull-up resistor on each I/O pin. These pull-up resistors can be controlled by user's program through RPC. When the corresponding control bit (rpc_n,) is enabled, the resistor will be active in input mode. In case of group interrupt input is set by mask option, the pull-up resistors on Port C are controlled by the mask option of interrupt polarity. Setting rising-edge trigger interrupt on PC7:0 will disable all pull-up resistors. If PC7:0 are configured as falling-edge trigger interrupt inputs, the resistors on PC7:0 can be controlled by the register RPC.

Each I/O pin has Schmitt-Trigger input buffer for input mode. PC7:0 are open-drain outputs in output mode. Setting the direction bit (dpc_n,) to "1" with the corresponding data bit (c_n,) to "0" will activate the pad as low. Once the data bit is changed to "1", the I/O pad will become tri-state.

PC7:0 are utilized as external interrupt inputs. More details will be described in ***Interrupt Chapter***.

The pad assignment for SPCP02A is as follows (VDD = 5.0V):

PIN	Rp		IN	OUT	Special Function
PC7	20K	Pull-up @ rpc7	Schmitt-Trigger	-/4mA	IRQ2 interrupt input
PC6	20K	Pull-up @ rpc6	Schmitt-Trigger	-/4mA	IRQ2 interrupt input
PC5	20K	Pull-up @ rpc5	Schmitt-Trigger	-/4mA	IRQ2 interrupt input
PC4	20K	Pull-up @ rpc4	Schmitt-Trigger	-/4mA	IRQ2 interrupt input
PC3	20K	Pull-up @ rpc3	Schmitt-Trigger	-/4mA	IRQ2 interrupt input
PC2	20K	Pull-up @ rpc2	Schmitt-Trigger	-/4mA	IRQ2 interrupt input
PC1	20K	Pull-up @ rpc1	Schmitt-Trigger	-/4mA	IRQ2 interrupt input
PC0	20K	Pull-up @ rpc0	Schmitt-Trigger	-/4mA	IRQ2 interrupt input

The definitions of mask options for Port C are:

Option	Relation	Description
aipc	PC7:0	*Alternative Input Option on PC for IRQ2.* Disable or Enable.
ippc	PC7:0	*Polarity Control Option of Interrupt Input on Port C.* Active Low or Falling Edge Trigger, or Active High or Rising Edge Trigger.

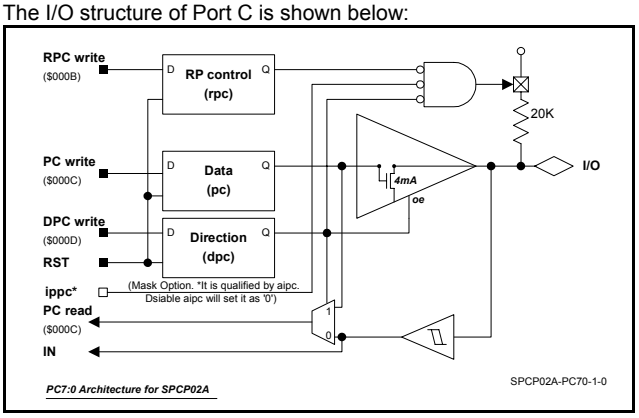
The definitions of registers PC, DPC, and RPC are showed below:

PC	Port C Data Register			$000C
Name	**Bit**	**RW**	**Dft**	**Functional Description**
c7:0	7:0	A	0h	*Port C Data*. When Port C is programmed as output, the output data on Port C pins are determined by PC data register. When Port C is programmed as input, any "read" command on Port C Data Register will reflect the logic status of I/O pins. PC data register will be set to "0" when RESET occurred.

DPC	Port C Data Direction Register			$000D
Name	**Bit**	**RW**	**Dft**	**Functional Description**
dpc7:0	7:0	W	0h	*Port C Data Direction*. Port C can be programmed as inputs or outputs by DPC register. When dpcn="1", the corresponding pins are programmed as outputs. When dpcn="0", the corresponding pins are programmed as inputs. The DPC will be set to "0"(input) when RESET occurred.

RPC	Port C Pull-up Control Register			$000B
Name	**Bit**	**RW**	**Dft**	**Functional Description**
rpc7:0	7:0	W	0h	*Port C Pull-up Disable*. When the bit is "0", the built in pull-up resistor of the corresponding pin in input mode will be enabled. When it is "1", the pull-up resistor will be disabled. The pull-up resistors are invalid during output mode. The RPC will be set to "0"(enable mode) by RESET.

The I/O structure of Port C is shown below:



5.8. Port D Group

The I/O Port D has 4 programmable I/Os that are controlled by data register (PD), direction control register (DPD), and pull-up resistance control register (RPD). DPD controls the pad I/O attribute. Setting the bit(s) to "1" will enforce the corresponding pad(s) to output mode. It is a write-only register. PD stores the data contents for output. Reading PD will get the stored data when corresponding bit of DPD is set as output mode, or will get the pad status if it is in input mode.

There is a built-in pull-up resistor on each I/O pin. These pull-up resistors can be controlled by user's program through RPD. When the corresponding control bit (rpd_n,) is enabled, the resistor will be activated in input mode. Each I/O pin has Schmitt-Trigger input buffer for input mode. PD3:0 are open-drain outputs in output mode. Setting the direction bit (dpd_n,) to "1" with the corresponding data bit (d_n,) to "0" will activate the pad as low. Once the data bit is changed to "1", the I/O pad will become tri-state. The output of PD can be used as LED sink output.

The pad assignment for SPCP02A is as follows (VDD = 5.0V):

PIN	Rp	IN	OUT	Special Function
PD3	100K Up @ rpd3	Schmitt-Trigger	-/12mA @ V_{OL} = 3.2V	nLED3 sink output
PD2	100K Up @ rpd2	Schmitt-Trigger	-/12mA @ V_{OL} = 3.2V	nLED2 sink output
PD1	100K Up @ rpd1	Schmitt-Trigger	-/12mA @ V_{OL} = 3.2V	nLED1 sink output
PD0	100K Up @ rpd0	Schmitt-Trigger	-/12mA @ V_{OL} = 3.2V	nLED0 sink output

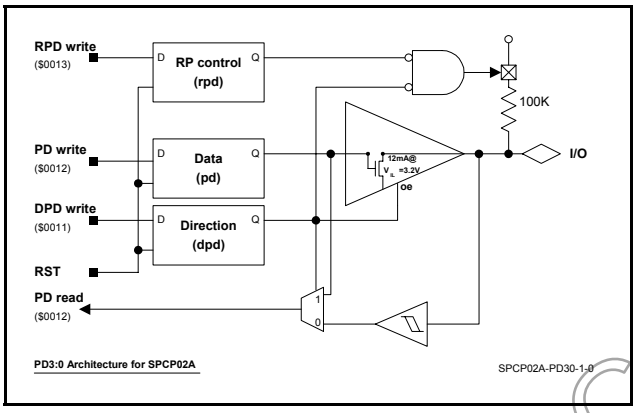
The definitions of registers PD, DPD, and RPD are showed below:

PD	Port D Data Register			$0012
Name	**Bit**	**RW**	**Dft**	**Functional Description**
resv.	7:6	-		*Reserved.*
	5:4	W		*Refer to Section Specific Shadow Register for more information.*
d3:0	3:0	A	0h	*Port D Data*. When Port D in programmed as output, the output data on Port A pins are determined by PD data register. When Port D is programmed as input, any "read" command on Port D Data Register will reflect the logic status of I/O pins. PD data register will be set to "0" when RESET occurred.

DPD	Port D Data Direction Register			$0011
Name	**Bit**	**RW**	**Dft**	**Functional Description**
	7:4	R	0h	*Refer to Section Reset for more information.*
dpd3:0	3:0	W	0h	*Port D Data Direction*. Port D can be programmed as inputs or outputs by DPD register. When **dpd**n="1", the corresponding pins are programmed as outputs. When **dpd**n="0", the corresponding pins are programmed as inputs. The DPD will be set to "0"(input) when RESET occurred.

RPD	Port D Pull-up Register			$0013
Name	**Bit**	**RW**	**Dft**	**Functional Description**
resv.	7:4	-		*Reserved.*
rpd3:0	3:0	W	0h	*Port D Pull-up Disable*. When the bit is "0", the built in pull-up resistor of the corresponding pin in input mode will be enabled. When it is "1", the pull-up resistor will be disabled. The pull-up resistors are invalid during output mode. The RPD will be set to "0"(enable mode) by RESET.

The I/O structure of Port D is shown below:



5.9. Port E Group

The I/O Port E has 4 programmable I/Os that are controlled by data register (PE,) direction control register (DPE), and pull-up/down resistance control register (RPE). DPE controls the pad I/O attribute. Setting the bit(s) to "1" will enforce the corresponding pad(s) to output mode. It is a write-only register. PE stores the data contents for output. Reading PE will get the stored data when corresponding bit of DPE is set as output mode, or will get the pad status if it is in input mode.

There is a built-in pull-up resistor on each pad. These pull-up resistors can be controlled by user's program through RPE. When the corresponding control bit (rpe_n,) is enabled, the resistor will be activated in input mode. Each I/O pin has Schmitt-Trigger input buffer for input mode. PE3:0 are open-drain outputs in output mode. Setting the direction bit (dpe_n,) to "1" with the corresponding data bit (e_n,) to "0" will activate the pad as low. Once the data bit is changed to "1", the I/O pad will become tri-state.

In 40-pin package, PE3:2 are not present. The values of the correlated data bits or control bits must be kept as the reset default.

The pad assignment for SPCP02A is as follows (VDD = 5.0V):

PIN	Rp	IN	OUT	Special Function
PE3	5K Up @ rpa3	Schmitt-Trigger	-/8mA	-
PE2	5K Up @ rpa2	Schmitt-Trigger	-/8mA	-
PE1	5K Up @ rpa1	Schmitt-Trigger	-/8mA	-
PE0	5K Up @ rpa0	Schmitt-Trigger	-/8mA	-

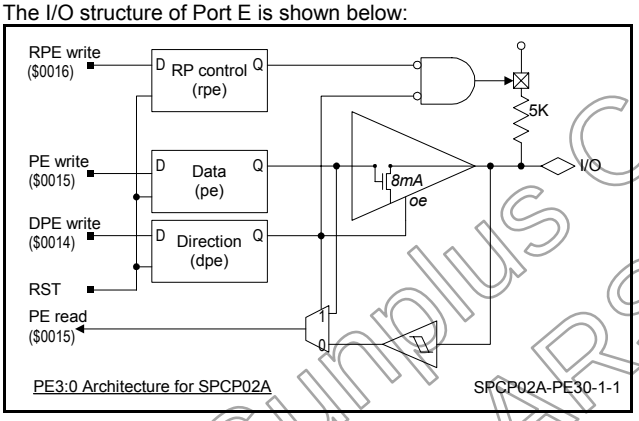
The definitions of registers PE, DPE, and RPE are shown below:

PE	Port E Data Register			$0015
Name	**Bit**	**RW**	**Dft**	**Functional Description**
resv.	7:4	-		*Reserved.*
e3:0	3:0	A	0h	*Port E Data*. When Port E is programmed as output pins, the output data on Port A pins are determined by PE data register. When Port E is programmed as input pins, any "read" command on Port E Data Register will reflect the logic status of those I/O pins. PE data register will be set to "0" when RESET occurred.

DPE	Port E Data Direction Register			$0014
Name	**Bit**	**RW**	**Dft**	**Functional Description**
resv.	7:4	-		*Reserved.*
dpe3:0	3:0	W	0h	*Port E Data Direction*. Port E can be programmed as inputs or outputs by DPE register. When **dpe**n="1", the corresponding pins are programmed as outputs. When **dpe**n="0", the corresponding pins are programmed as inputs. The DPE will be set to "0"(input) when RESET occurred.

RPE	Port E Pull-up/down Register			$0016
Name	**Bit**	**RW**	**Dft**	**Functional Description**
resv.	7:4	-		*Reserved.*
rpe3:0	3:0	W	0h	*Port E Pull-u Disable*. When the bit is "0", the built in pull-up resistor of the corresponding pin in input mode will be enabled. When it is "1", the resistor will be disabled. The resistors are invalid during output mode. The RPE will be set to "0"(enable mode) by RESET.

The I/O structure of Port E is shown below:



5.10. Port F Group

The I/O Port F has 8 programmable I/Os that are controlled by data register (PF), direction control register (DPF), and pull-up/down resistance control register (RPF). DPF controls the pad I/O attribute. Setting the bit(s) to "1" will enforce the corresponding pad(s) to output mode. It is a write-only register. PF stores the data contents for output. Reading PF will get the stored data when corresponding bit of DPF is set as output mode, or will get the pad status if it is in input mode.

There is a built-in pull-up resistor on each I/O channel. These pull-up resistors can be controlled by users' program through RPF. When the corresponding control bit (rpf_n,) is enabled, the resistor will be activated in input mode. Each I/O pin has Schmitt-Trigger input buffer for input mode. PF7:0 are open-drain outputs in output mode. Setting the direction bit (dpf_n,) to "1" with the corresponding data bit (f_n,) to "0" will activate the pad as low. Once the data bit is changed to "1", the I/O pad will become tri-state.

The pad assignment for SPCP02A is as follows (VDD = 5.0V:)

PIN	Rp	IN	OUT	Special Function
PF7	100K Up @ rpa7	Schmitt-Trigger	-/4mA	-
PF6	100K Up @ rpa6	Schmitt-Trigger	-/4mA	-
PF5	100K Up @ rpa5	Schmitt-Trigger	-/4mA	-
PF4	100K Up @ rpa4	Schmitt-Trigger	-/4mA	-
PF3	100K Up @ rpa3	Schmitt-Trigger	-/4mA	-
PF2	100K Up @ rpa2	Schmitt-Trigger	-/4mA	-
PF1	100K Up @ rpa1	Schmitt-Trigger	-/4mA	-
PF0	100K Up @ rpa0	Schmitt-Trigger	-/4mA	-

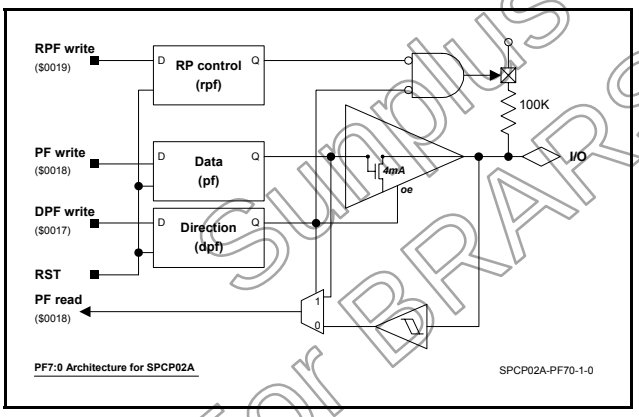
The definitions of registers PF, DPF, and RPF are shown below:

PF	Port F Data Register			$0018
Name	**Bit**	**RW**	**Dft**	**Functional Description**
f7:0	7:0	A	0h	*Port F Data*. When Port F is programmed as output pins, the output data on Port F pins are determined by PF data register. When Port F is programmed as input pins, any "read" command on Port F Data Register will reflect the logic status of I/O pins. PF data register will be set to "0" when RESET occurred.

DPF	Port F Data Direction Register			$0017
Name	**Bit**	**RW**	**Dft**	**Functional Description**
dpf7:0	7:0	W	0h	*Port F Data Direction*. Port F can be programmed as inputs or outputs by DPF register. When **dpf**n="1", the corresponding pins are programmed as outputs. When **dpf**n="0", the corresponding pins are programmed as inputs. The DPF will be set to "0"(input) when RESET occurred.

RPF	Port F Pull-up Control Register			$0019
Name	**Bit**	**RW**	**Dft**	**Functional Description**
rpf7:0	7:0	W	0h	*Port F Pull-up Disable*. When the bit is "0", the built in pull-up resistor of the corresponding pin in input mode will be enabled. When it is "1", the pull-up resistor will be disabled. The pull-up resistors are invalid during output mode. The RPF will be set to "0"(enable mode) by RESET.

The I/O structure of Port F is shown below:



5.11. Interrupt

There are four types of interrupts: Software Interrupt, External Interrupt, Timer Interrupt, and Comparator interrupt. The last three interrupts has individual status (occurred or not occurred) and control (enable or not enabled) registers. In contrast, software interrupt does not have these control registers. In general, once an interrupt event occurs, the corresponding flag bit will be set. If the related interrupt control bit is enabled, an interrupt request signal will be generated and be executed by CPU. The interrupt flag bits must be cleared in the interrupt service routine to avoid program from deadlock in interrupt service routine.

Software interrupt is generated by the instruction BRK. The BRK is an executable instruction interrupt; it is executed regardless of the state of the I-bit in the Processor Status Register Flag (inside CPU). The program jumps to interrupt routine immediately when BRK occurred. With any instruction, interrupts pending during the previous instruction is served.

External interrupts come from IRQ0 or IRQ2. These IRQ signals are combined with the mask options and status/control registers to generate the interrupt events to CPU. IRQ0 has an interrupt control bit (**irqe**) to enable the interrupt generating, a write-only clear bit (**irqr)** to clear occurred event status, and a read-only flag bit (**irqf**) for get event status. Once an external interrupt is occurred, **irqf** will be set and it stays set unless the **irqr** is set to "1" by user's program. When setting **irqe** to enable IRQ0, an interrupt request signal will be generated as long as **irqf** is set. IRQ2 has only one interrupt control bit (**irqe2**) and one flag bit (**irqf2)**. Clearing **irqe2** will disable the IRQ2. IRQ0 has mask option used in setting the trigger mode of the interrupt event. The trigger mode of IRQ0 can be selected as either edge trigger mode or level trigger mode. On the other hand, IRQ2 only has edge trigger mode. When the interrupt channel is enabled with edge trigger mode, an active transition edge on the external interrupt inputs will generate the interrupt. If the channel is enabled with level trigger mode, the active level of the external interrupt inputs will set the interrupt event until the active level condition is removed. However, user's program must set related **irqr**n bit to

clear the interrupt occurrence in the interrupt service routine.

In SPCP02A, IRQ0 comes from PB5, and IRQ2 comes from external interrupt group input, PC7:0. Each IRQ channel has a mask option for input control of the interrupt, and a mask option for interrupt polarity. The mask options of input control activates the interrupt input on PB5 or PC7:0. For interrupt polarity, the mask options can be set as rising-edge trigger or falling-edge trigger for the IRQ channels.

When the interrupt input is enabled by the mask option, the control of pull-up resistor(s) will be affected by the mask option of interrupt polarity in case of the option is set as rising-edge trigger (or active high trigger). If the interrupt polarity is set as rising-edge trigger (or active high trigger), the pull-up resistor(s) will be disabled permanently.

The Timer 1 interrupt and the Comparator interrupt will be described in section Timer1 & Real Time Interrupt and section Comparator.

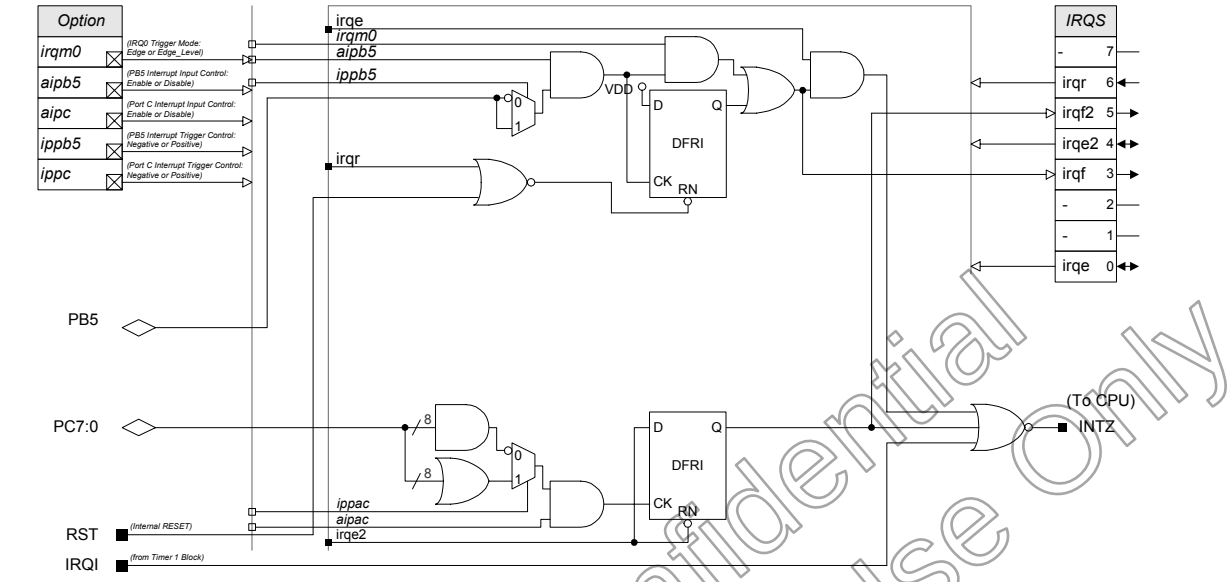
The definitions of mask options for external interrupts are:

Option	Relation	Description
irqm0	IRQ0	*IRQ Trigger Mode Option on IRQ0.* Edge Trigger or Level-Edge Trigger.
aipb5	IRQ0, PB5	*Alternative Input Option on PB5 for IRQ0.* Alternative input is disabled or enabled. The polarity control function of ippb5 is ignored when aipb5 is disabled. It controls the input PB5 for IRQ0.
aipc	IRQ2, PC7:0	*Alternative Input Option on PC for IRQ2.* Alternative Input is disabled or enabled. The polarity control function of ippc is ignored when aipc is disabled. It controls the group input PC7:0 for IRQ2.
ippb5	IRQ0, PB5	*Polarity Control Option of Interrupt Input on PB5.* Falling edge trigger or rising edge trigger. It controls the polarity of interrupt input on PB5. When aipb5 is disabled, this option is ignored. When it is effective with value '1', the internal Pull-up Resistor on PB5 is disabled.
ippc	IRQ2, PC7:0	*Polarity Control Option of Interrupt Input on PC.* Falling edge trigger or rising edge trigger. It controls the polarity of interrupt input on PC and it does affect the pull-up/down resistors on all PC pins when the alternative input is enabled by aipc. If the option is set '1', all PC pull-up resistors are disabled. In case of setting this bit to '"0", the resistors are not affected by the option.

The control register for external interrupt inputs is defined in detail as below:

IRQS				IRQ Control & Status Register	$0006
Name	**Bit**	**RW**	**Dft**	**Functional Description**	
resv.	7	-		*Reserved.*	
irqr	6	W		***Irqf** Clear bit*. It clears flag ***irqf***. Writing "1" to ***irqr*** will clear flag ***irqf***. 0: not clear, 1: clear ***irqf***.	
irqf2	5	R	0	*Interrupt Flag bit of IRQ2 Input*. It indicates the interrupt requests coming from channel IRQ2. The flag is set by the interrupt events and is cleared by setting **irqe2** to "0". The IRQ2 is from PC7:0. 0: no interrupt, 1: interrupt requested.	
irqe2	4	A	0	*Interrupt Control bit of IRQ2 Input*. It controls whether the interrupt requests comes from IRQ2. 0: disable, 1: enable.	
irqf	3	R	0	*Interrupt Flag bit of IRQ0 Input*. It is the flag of interrupt requests coming from channel IRQ0. The flag is set by the interrupt events and is cleared by setting **irqr** to "1". Setting **irqe** does not affect **irqf**. IRQ0 comes from PB5. 0: no interrupt, 1: interrupt requested.	
resv.	2:1	-		*Reserved.*	
irqe	0	A	0	*Interrupt Control bit of IRQ0 Input*. It controls whether the interrupt requests comes from IRQ0. 0: disable, 1: enable.	

The interrupt source diagrams in different emulation modes are shown below:



Interrupt Architecture for SPCP02A

SPCP02A-INTR-1-1

5.12. Timer1 & Real Time Interrupt

The clock input (XI/XO/R pins), f_{OSC}, is internally divided by two to generate the CPU clock (f_{CPU}) for entire system. Timer 1 clock (f_{TM1}) comes from CPU clock with the division of 1 or 4, configured by mask option. The timer clock is fed into an 8-bit free-run timer built as Timer 1 function. Timer 1 Count Register (TCR1) reads the current counting value of Timer 1. Once TCR1 overflows, it will set the interrupt flag bit **tof1** of Timer 1 Control & Status Register (TCS1) to "1" and will generate interrupt for service if the interrupt enable bit (**tofe1)** of TCS1 is set. Writing the write-only bit (**tofr1)** of TCS1 with "1" clears the flag.

The additional counting stages perform the Real Time Interrupt (RTI) function for timing applications, the watchdog Timer for function recovery, and the Power On Reset (POR) cycle for lowing clock during power up. More information about the POR and WDT functions are described in ***WDT & Reset Chapter***.

Real Time Interrupt (RTI) comes from the additional counting stages. Some of these additional counting stages consist of a pre-scalar to perform the periodic timing events. The timing events will set the flag bit (**rtif**) in TCS1 and will generate interrupt for service if the interrupt enable bit (**rtie)** of TCS1 is set. Writing the write-only bit (**rtifr)** of TCS1 with "1" clears the flag. The rt1 and rt0 of TCS1 select the division for pre-scalar. The corresponding definitions are described as follows.

The definition of mask option for Timer1 & Real Time Interrupt is:

Option	Relation	Description
fsel	Timer1	Timer 1 Clock Divisor. 0: f_{CPU}/1. 1: f_{CPU} /4.

The control register for external interrupt inputs is defined in details as below:

TCR1	Timer Counter Register 1			$0005
Name	**Bit**	**RW**	**Dft**	**Functional Description**
tm1r7:0	7:0	R	0	*Timer Counter Register 1*. This register is a read-only register. It reports the current value of the beginning 8-bit of timer chain. It is cleared by reset.

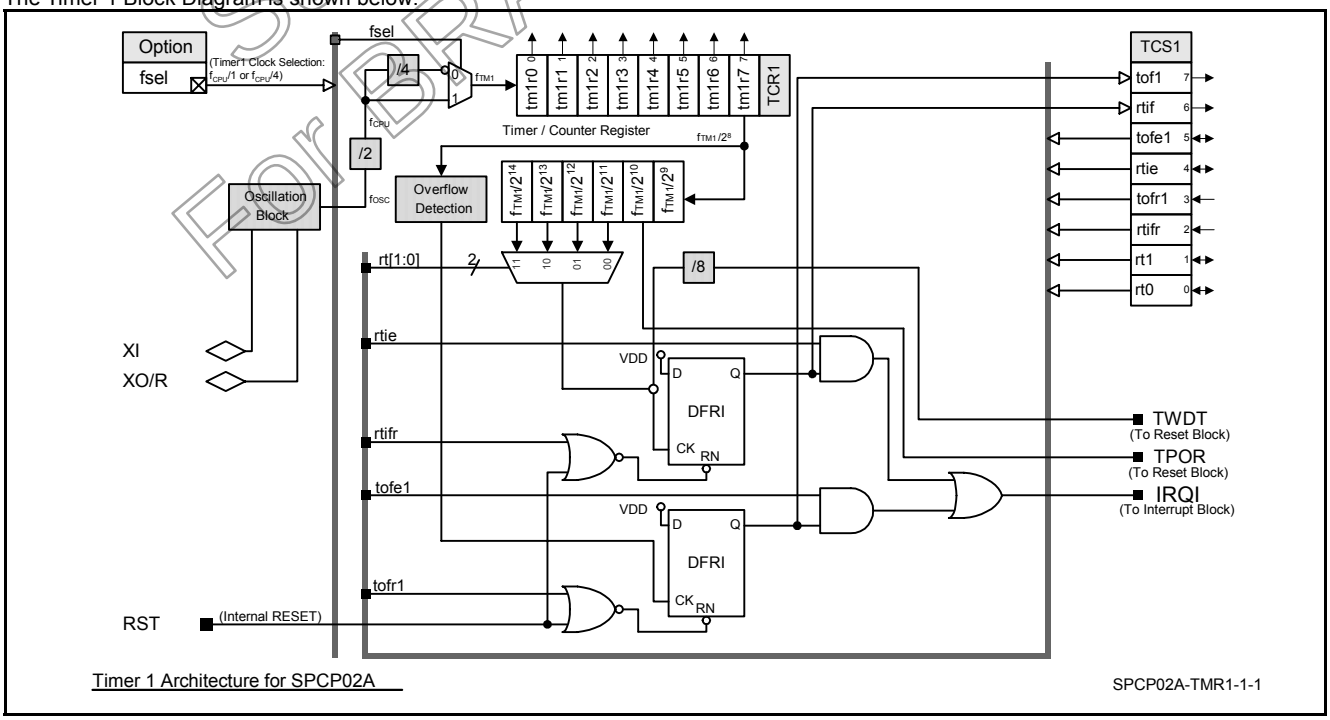
TCS1	Timer Control/Status Register 1			$0004
Name	**Bit**	**RW**	**Dft**	**Functional Description**
tof1	7	R	0	*Overflow Flag bit of Timer 1*. It indicates the TCR1 rolling over from $FF to $00. 0: no overflow, 1: overflow is set. It can be cleared by writing "1" to **tofr1**.
rtif	6	R	0	*Real Time Interrupt Flag bit of Timer 1*. It indicates the status of selected Real Time Interrupt Event of TCR1. 0: no event, 1: event is set. It can be cleared by writing "1" to **rtifr**.
tofe1	5	A	0	*Overflow Interrupt Control bit of Timer 1*. It controls whether the interrupt event is generated by **tof1**. 0: interrupt disable, 1: interrupt enable.
rtie	4	A	0	*Real Time Interrupt Control bit of Timer 1*. It controls whether the interrupt event of selected Real Time is generated by **rtif**. 0: interrupt disable, 1: interrupt enable.
tofr1	3	W		*Overflow Interrupt Clear bit of Timer 1*. It clears **tof1** by writing "1" to this bit. 0: not cleared, 1: clear.
rtifr	2	W		*Real Time Interrupt Clear bit of Timer 1*. It clears **rtif** by writing "1" to this bit. 0: not cleared, 1: clear.
rt1:0	1:0	A	11	*Selection of Real Time Interrupt Rate*. It selects the Interrupt rate for Timer 1. The related rate is shown below.

rt1:0	RTI Rate			WDT Reset time (=RTI/8)		
	Divisor	$f_{TM1}=f_{CPU}/1$*	$f_{TM1}=f_{CPU}/4$*	Divisor	$f_{TM1}=f_{CPU}/1$*	$f_{TM1}=f_{CPU}/4$*
00	2048	2.048ms	8.192ms	16384	16.384ms	66ms
01	4096	4.096ms	16.384ms	32768	32.768ms	131ms
10	8192	8.192ms	32.768ms	65536	66ms	262ms
11	16384	16.384ms	65.536ms	131072	131ms	524ms

Note1: In this example, the CPU clock is f_{CPU} = 1.0MHz that comes from the oscillation clock base f_{OSC} = 2.0MHz.

Note2: *The f_{TM1} is selected by mask option ***fsel***.

The Timer 1 Block Diagram is shown below:



Timer 1 Architecture for SPCP02A

SPCP02A-TMR1-1-1

5.13. STOP Mode

There is a clock control modes supported by SPCP02A as STOP mode.

The STOP mode function will disable the entire system clock if the bit **stop** is set to "1". Once the system enters the STOP mode, only the activated external interrupt events (from I/Os) are able to recover the normal operation from the next address of STOP mode interrupt point with 1024 f_{TM1} clock cycle recovery time for stable oscillation. To confirm the external interrupt events are able to wake the system up, the corresponding interrupt enable bits must be set before entering the STOP mode. There is an option named xxxx to disable the STOP mode for EMS improvement. Setting the option to disable the STOP mode will inhibit the bit being set to '1'.

The definitions of mask options for STOP mode is:

Option	Relation	Description
nosnw	STOP	*STOP mode Control.* Enable STOP mode or Disable STOP mode.

The control register for Comparator function is defined in detail as below:

SNW	STOP & WAIT Mode Control Register			0008$
Name	**Bit**	**RW**	**Dft**	**Functional Description**
resv.	7:5	-		*Reserved.*
stop	4	W		*Stop Mode Selection*. It sets the micro-controller entering the STOP mode. CPU clock and Timer counter is disabled when it is set to "1". Only one of the external interrupts can resume the micro-controller back to normal operation from next address of STOP mode interrupt pointer.
resv.	3:0	-		*Reserved.*

5.14. Reset

There are five reset resources in SPCP02A -- Power On Reset (POR), External Reset (PB4), Low Voltage Reset (LVR), Watchdog Timer Reset (WDT), and Illegal Address Reset (IAR).

Power on Reset is an internal reset. During the power up cycle, the POR reset cycle is extended 50ms in minimum and up to 300ms in maximum from system reset. The extension cycle provides a delay for oscillator stabilization. The period of extension cycle depends on the mask option of Timer1 clock divisor. The extended period for divisor as 4 is 4 times of the period for divisor as 1. To confirm the Power on Reset is generated properly, the system VDD should be held at a zero potential with respect to ground. Improper initial setting of the VDD may cause the Power on Reset failure, which yields improper initialization. If the external RESET pin (PB4) is enabled and is low at the end of this extension, CPU remains in the reset-state until RESET goes high. The user must ensure that the voltage on VDD has risen to a point where the MCU can operate properly by the time of POR has elapsed. If there is doubt, the external RESET pin should enable and remain low until the voltage on VDD has reached the specified minimum operating voltage. This may be accomplished by connecting an external RC circuit to this pin to generate a power-on reset (POR). In this case, the time constant must be large enough to stabilize the oscillator circuit.

PB4 can be selected as an I/O with external reset input by mask option. When it is configured as an I/O with external reset input, it will activate reset cycle by holding the pin as low in input mode. This pin is connected to an internal Schmitt trigger input. Once the pin is selected with reset function, setting the direction of this pin as input with enabling the pull-up resistor is recommended. Improper setting in the transition between input mode and output mode of PB4 may cause the unexpected reset cycle.

Internal Low Voltage Reset is generated when VDD falls below the specific LVR trigger voltage for at least one clock cycle. A mask option is used to enable or disable the function.

The Watchdog Timer (WDT) can be disabled or enabled through mask option. The internal reset of WDT will be generated by a time-out of the WDT automatically when watchdog is enabled. It is implemented on this device using the output of the RTI circuit and further dividing it by eight (RT1, RT0 timing times 8). This time out generates reset if the WDT register is not cleared. An internal reset is generated to restart the system. Writing "1" to **wdt** (bit 0 of CPWD) does prevent a WDT time-out reset within a specific time. The minimum WDT reset time is listed in section Timer1 and Real Time Interrupt.

The internal reset of IAR is generated when an instruction op-code fetch occurs from an address not in the working area ($0000-$1FFF). The IAR will generate the reset signal that will reset the CPU and other peripherals.

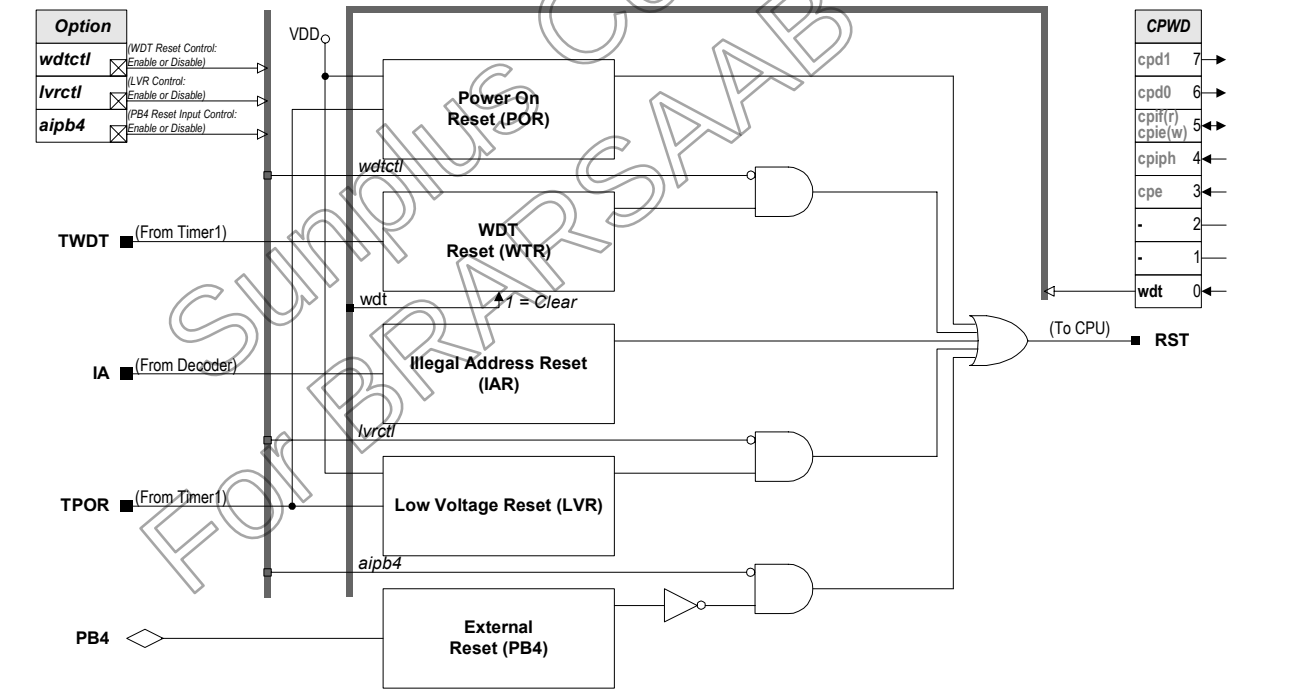
The definitions of mask options for Reset are:

Option	Relation	Description
wdtctl	WDT	*Watchdog Timer Reset Control Option.* Enabled or Disabled.
lvrctl	LVR	*Low Voltage Reset Control Option.* Enabled or Disabled.
aipb4	RESET, PB4	*Alternative Input Option on PB4 for Reset.* PB4 is an I/O with external Reset input, or it is a general I/O without external reset input.

The control bit for Watchdog Timer Reset function is located in CPWD and is defined in details as below:

CPWD	Comparator & WDT Control/Status Register			$0007
Name	**Bit**	**RW**	**Dft**	**Functional Description**
	7:1			Please refer to ***Comparator Chapter*** for more detail.
wdt	0	W		*Watch Dog Timer Clear bit*. It clears the watchdog timer time-out event for reset function in write mode. 0: not cleared, 1: clear.

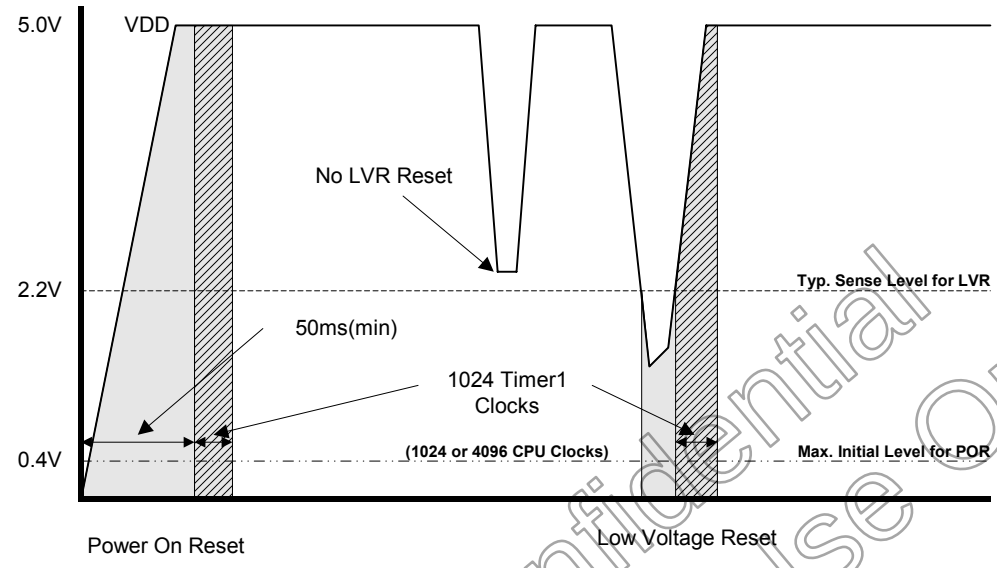
The RESET Block Diagram is shown below:



RESET Architecture for SPCP02A

SPCP02A-RST-1-1

The Reset Timing is shown below:



RESET Architecture for SPCP02A

SPCP02A-RST-1-1

5.15. Special Shadow Register

In case of the specific application, there is a special shadow register, SSR, being built in to maintain the reset condition by the firmware. The high nibble of the SSR has two bits to report the error status of the CPU, and two custom-specific bits for the convenience of the applications. The high nibble of the SSR is located in the **pd7:4** in the write cycle. A read cycle of PD register does not enable the SSR to report the data to avoid conflict. It can be read back from the same address of the register DPD. However, this register is reset only when the power is turned on. The definition detail is described below:

SSR	Specific Shadow Register – High Nibble Write				$0012
Name	**Bit**	**RW**	**Dft**	**Functional Description**	
resv.	7:6	-		*Reserved.*	
ssr1:0	5:4	W		*Customer Specific Bit 1:0.* It is used as an indicator for the customer's application. However, it is written through $0012h, but it is read from $0011h.	
	3:0	-		*Refer to Section Port D for more information.*	

SSR	Specific Shadow Register – Read				$0011
Name	**Bit**	**RW**	**Dft**	**Functional Description**	
iadr	7	R	0	*Illegal Address Status.* It indicates an error occurred for the illegal address. 0: No error, 1: Error is occurred. The status is reset only when the power is turned on or a write cycle of PD.	
oper	6	R	0	*OP Code Error Status.* It indicates an error occurred for the OP code errors. 0: No error, 1: Error is occurred. The status is reset only when the power is turned on or a write cycle of PD.	
ssr1:0	5:4	R	0	*Customer Specific Bit 1:0.* It is used as an indicator for the customer's application. It is reset only when the power is turned on. However, it is written through $0012h, but it is read from $0011h.	
	3:0	-		*Refer to **Port D** for more information.*	

5.16. Mask Options

The mask options are used to setup the operation condition. The definitions are summarized below:

Name	Relation	Function
aipb5	PB5	*Alternative Input Option on PB5 for IRQ0.* Alternative Input is disabled or enabled. The polarity of IRQ0 input on PB5 is fixed as Active Low or Falling Edge Trigger.
aipb4	PB4	*Alternative Input Option on PB4 for nRESET.* Alternative Input is enabled or disabled.
aipc	PC7:0	*Alternative Input Option on PC for IRQ2.* Alternative Input is Disabled or Enabled. The polarity control function of ippc is ignored when aipc is disabled.
ippb5	PB5 Pin	*Polarity Control Option of Interrupt Input on PB5.* It selects the polarity of interrupt input on PB5. 0 either Active Low or Falling Edge Trigger, or Active High or Rising Edge Trigger. It does affect the pull-up resistor on PB5 when the alternative input is enabled by aipb5. If the option is set as rising edge trigger, the pull-up resistor is disabled.
ippc	PC7:0 Pin	*Polarity Control Option of Interrupt Input on Port C.* It selects the polarity of interrupt input on Port C either Active Low or Falling Edge Trigger, or Active High or Rising Edge Trigger. It is ignored when aipc is disabled. It controls the polarity of interrupt input on PC and does affect the pull-up/down resistors on all PC pins when the alternative input is enabled by aipc. If the option is set as rising edge trigger, all of the PC pull-up resistors are disabled. In case of setting this bit to falling edge trigger, the resistors are not affected by the option.
odpb7:4	PB7:4 Pin	*Open Drain Output Option on PB7:4.* Open-Drain Output or Totem-Pole Output.
irqm0	IRQ0	*IRQ Trigger Mode Option on IRQ0.* Edge Trigger or Level-Edge Trigger.
nosnw	STOP	*STOP mode Control.* Enable STOP mode or Disable STOP mode.
clkext	XI/XO	*External Clock Input Option.* This option is combined with the option oscm to select the oscillation mode. Three oscillation modes can be selected: External Clock input Mode, Crystal/Resonator oscillation Mode, and External ROSC Mode.
oscm	XI/XO	*Oscillation Mode Option.* This option is combined with the option clkext to select the oscillation mode. Three oscillation modes can be selected: External Clock input Mode, Crystal/Resonator oscillation Mode, and External ROSC Mode.
fsel	Clock	*Timer1 Clock Divisor Option:* $f_{CPU}/1$ or $f_{CPU}/4$.
lvrctl	LVR	*Option of Function Control on Low Voltage Reset:* Enabled or Disabled.
wdtctl	WDT	*Option of Function Control on Watchdog Timer Reset:* Enabled or Disabled.
p40sel	PE[3:2], PB[7:6]	*Option for 40/44 pads selection.* Select 44 pads or 40 pads. When set it as 40 pads, PB[7:6] and PE[3:2] will be set to input mode, and the input data is gated as low.

6. ELECTRICAL SPECIFICATIONS

6.1. Item Definition

Item	Definition	Item	Definition
V_{IH}	Input High Voltage	I_{OH}	Output High Current (Source)
V_{IL}	Input Low Voltage	I_{OL}	Output Low Current (Sink)
V_{TH}	Input Threshold Voltage	I_Z	Output Leakage Current (Source)
SF_V	Frequency Stability	R_P	Pull-up/down Resistance
DF_V	Frequency Deviation		

6.2. Absolute Maximum Rating

Characteristics	Item	Min.	Typ.	Max.	Unit	Condition
Storage Temperature	T_{STR}	-40	-	125	°C	Sealed package
Operating Ambient Temperature	T_{OPR}	0	-	70	°C	
Voltage Rating on Input	V_{IN}	-0.3	-	VDD+0.3	V	
Voltage Rating on VDD		-0.3	-	7.0	V	
Output Voltage	V_{OUT}	0	-	VDD	V	

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

6.3. Recommended Operating Conditions

Characteristics	Item	Min.	Typ.	Max.	Unit	Condition
Operating Supply Voltage	VDD	2.4	-	5.5	V	
CPU Clock (Internal CPU clock)	f_{CPU}	200K	-	6.0M	Hz	VDD = 5.0V
Power Consumption	I_{DD}	-	4.0	-	mA	f_{CPU} = 6.0MHz @ VDD = 5.0V
Power Up Initial Voltage	V_{INIT}		-	0.5	V	
Power Up Cycle	t_{POR}	50	-	400	ms	VDD = 5.0V
LVR Trigger Voltage	V_{LVR}	-	2.2	-	V	

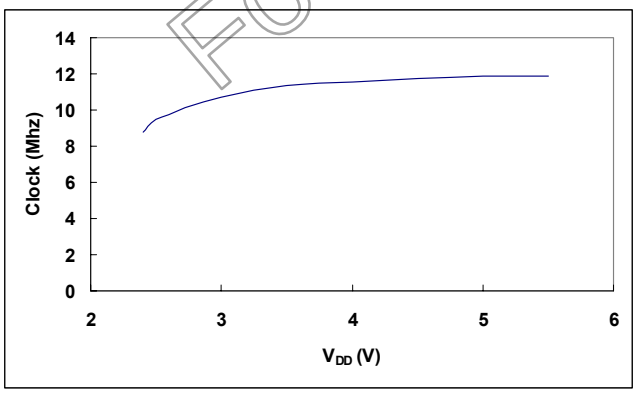
6.4. PIN Attribute Description (VDD = 5.0V, Temperature = 25ºC)

Mnemonic	Description	Item	Min.	Typ.	Max.	Unit	Condition
XI, XO	Special Input Cell Pair for RC oscillation	SF_V	-	-	±5.0	%	$(f_{5.5V}-f_{4.5V})/f_{5V}$ *
		DF_V	-	-	±10	%	TC = 25ºC
		R_P	-	27	-	KΩ	f_{CPU_5V} = 6MHz
PA7:0	Input Schmitt Trigger with	V_{IH}	2.0	-	-	V	
PB3:0	100KΩ Resistive Pull-up,	V_{IL}	-	-	0.8	V	
PF7:0	4mA Open-Drain Output	I_{OL}	4.0	-	-	mA	V_{OL} = 0.4V
		R_P	70	100	130	KΩ	V_{IN} = VSS
PB7:4	Input Schmitt Trigger with 100KΩ Resistive Pull-up, 4mA Output with Totem Pole or Open-Drain Option	V_{IH}	2.0	-	-	V	
		V_{IL}	-	-	0.8	V	
		I_{OH}	4.0	-	-	mA	V_{OH} = 2.0V
		I_{OL}	4.0	-	-	mA	V_{OL} = 0.4V
		R_P	70	100	130	KΩ	V_{IN} = VSS
PC7:0	Input Schmitt Trigger with 20KΩ Resistive Pull-up, 4mA Open-Drain Output	V_{IH}	2.0	-	-	V	
		V_{IL}	-	-	0.8	V	
		I_{OL}	4.0	-	-	mA	V_{OL} = 0.4V
		R_P	14	20	26	KΩ	V_{IN} = VSS
PD3:0	Input Schmitt Trigger with 100KΩ Resistive Pull-up, 12mA Open-Drain Output	V_{IH}	2.0	-	-	V	
		V_{IL}	-	-	0.8	V	
		I_{OL}	12	-	-	mA	V_{OL} = 3.2V
		R_P	70	100	130	KΩ	V_{IN} = VSS
PE3:0	Input Schmitt Trigger with 5KΩ Resistive Pull Up/down Option, 8mA Open-Drain Output	V_{IH}	2.0	-	-	V	
		V_{IL}	-	-	0.8	V	
		I_{OL}	8.0	-	-	mA	V_{OL} = 0.4V
		R_P	3.5	5.0	7.0	KΩ	V_{IN} = VSS
All	I/O Port Hi-Z Leakage	I_Z	-	-	10	μA	R_P inactive

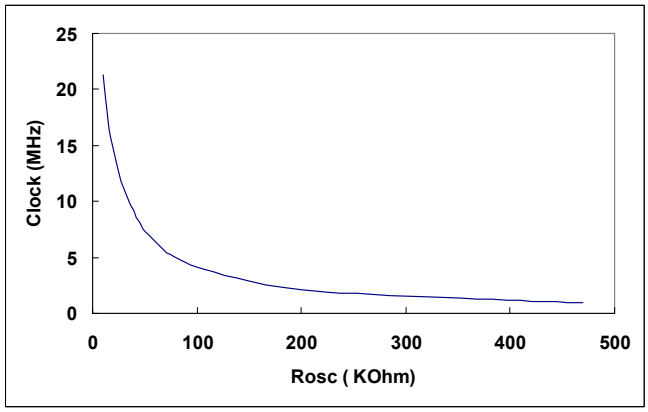
Note: *The frequency defined in this item is based on the CPU frequency. It is one-half of the oscillation frequency.

6.5. R-osc Frequency Reference Data

6.5.1. Frequency vs VDD (Temperature = 25ºC)



6.5.2. Frequency vs resistor value (VDD = 5.0V, Temperature = 25ºC)



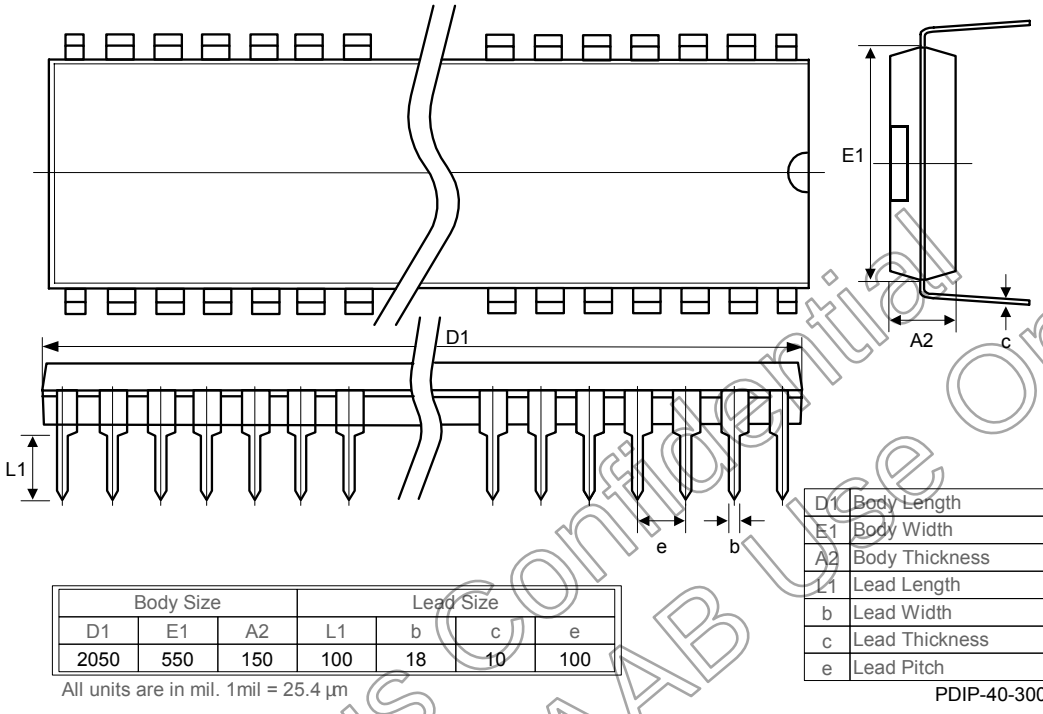
7. PACKAGE/PAD LOCATIONS

7.1. PAD Assignment and Locations

Please contact Sunplus sales representatives for more information.

7.2. Package Information

7.2.1. PDIP 40



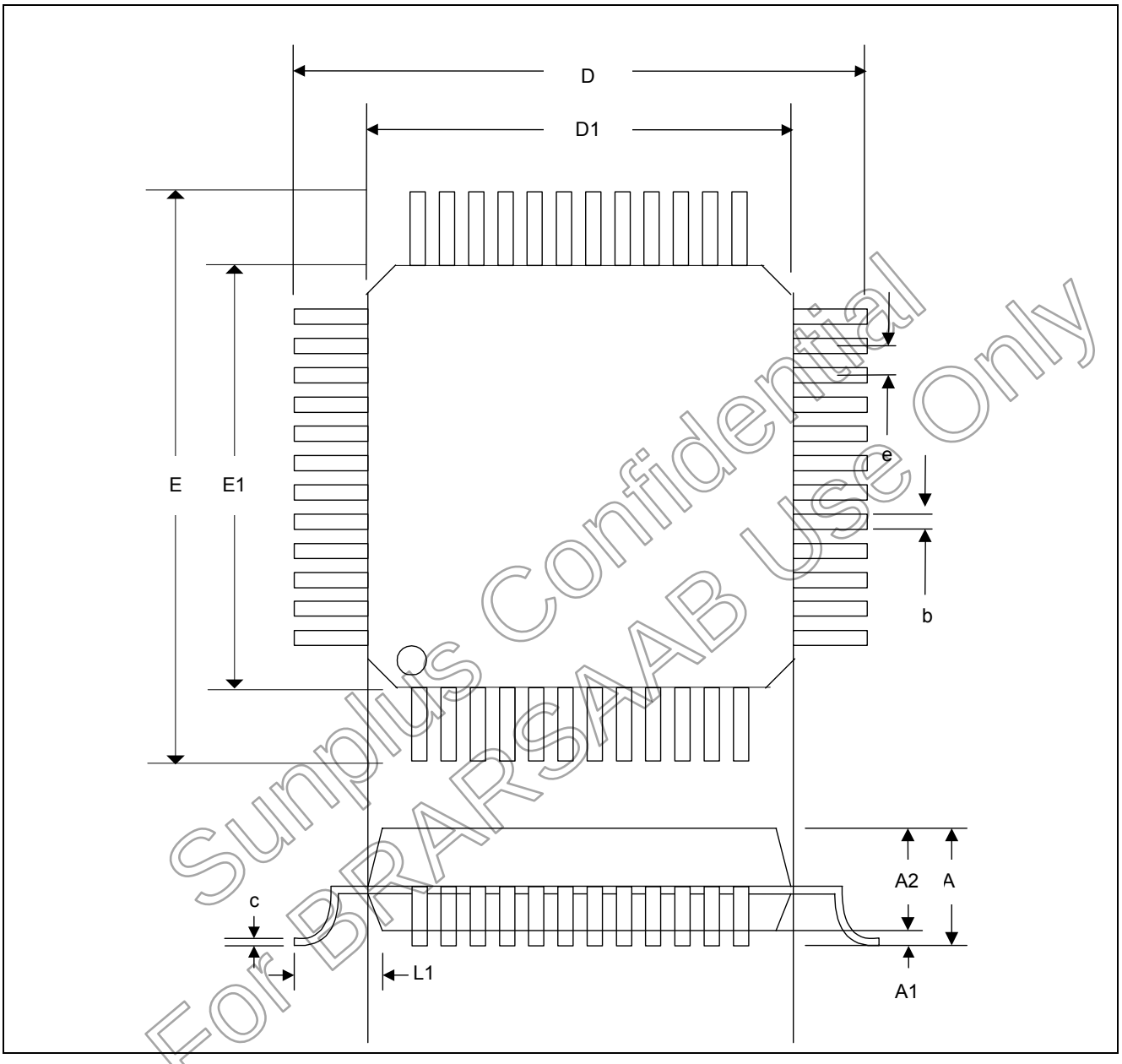
Body Size			Lead Size			
D1	E1	A2	L1	b	c	e
2050	550	150	100	18	10	100

All units are in mil. 1mil = 25.4 μm

D1	Body Length
E1	Body Width
A2	Body Thickness
L1	Lead Length
b	Lead Width
c	Lead Thickness
e	Lead Pitch

PDIP-40-300

7.2.2. LQFP 48



Symbol	Min.	Nom.	Max.	Unit
A	-	-	1.60	Millimeter
A1	0.05	-	0.15	Millimeter
A2	1.35	1.40	1.45	Millimeter
D		9.00 BSC		Millimeter
D1		7.00 BSC		Millimeter
E		9.00 BSC		Millimeter
E1		7.00 BSC		Millimeter
L1		1.00 REF		Millimeter
b	0.17	0.22	0.27	Millimeter
c	0.09	-	0.20	Millimeter
e		0.50 BSC		Millimeter

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9. REVISION HISTORY

Date	Revision #	Description	Page
AUG. 05, 2003	1.1	1. Add Package form - LQFP 48 Pin 2. Remove "*7.1 PAD Assignment and Locations*"	4, 5, 29 27
JUL. 18, 2002	1.0	1. Added the figure of frequency vs. R and frequency vs. VDD in section 6.5. 2. Revised the Pull up/down on PE3:0 as Pull-up only. Corrected the corresponding data including DC characteristics and option. 3. Corrected the figure of Memory mapping on RAM area from $0040-$00FF to $0060-$00FF. 4. Removed WAIT mode and corresponding content. 5. Removed option irqm2 and corresponding content. 6. Added new option nosnw for EMS improvement. 7. Corrected the output signal name from INTZ to RST in the figure of reset block diagram. 8. Correct "*7.2 Ordering Information*" 9. Delete "*PRELIMINARY*"	
SEP. 13, 2001	0.1	Original	30