

8T24 Line Receiver

Triple Line Receiver with Hysteresis
Product Specification

Logic Products

FEATURES

- Built-in input threshold hysteresis*
- High speed: $t_{PHL} = t_{PLH} = 20\text{ns}$ (typical)
- Each channel can be strobed independently
- Fanout of ten (10) with standard TTL integrated circuits
- Input gating is included with each line receiver for increased application flexibility
- Operation from a single +5V Power Supply

*Hysteresis is defined as the difference between the input thresholds for the "1" and "0" output states. Hysteresis is specified at 0.4V typically and 0.2V minimum over the operating temperature range.

DESCRIPTION

The 8T24 is a Triple Line Receiver designed specifically to meet the IBM System (360, System/370 I/O Interface Specification [IBM Specification GA 22-6974-0]): Each receiver incorporates hysteresis to provide high noise immunity and high input impedance to minimize loading on the driver circuit.

An input voltage of 1.7 volts or more is interpreted as a logical one; an input of

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
N8T24	20ns (t_{PLH})	
	20ns (t_{PHL})	

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$
Plastic DIP	N8T24N

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	8T
R	Input	4.3ul
S, A, B	Input	1ul
f	Output	8ul

NOTE:

A unit load (ul) is $40\mu\text{A } I_{IH}$ and $-1.6\text{mA } I_{IL}$.

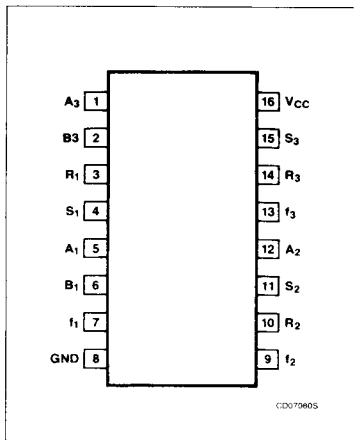
0.70 volts or less is interpreted as a logical zero as is an open circuited input.

The receiver input (R) of the 8T24 will not be damaged by a DC input of +7.0 volts with power on or by a DC input of +6.0 volts with power off in the receiver. The

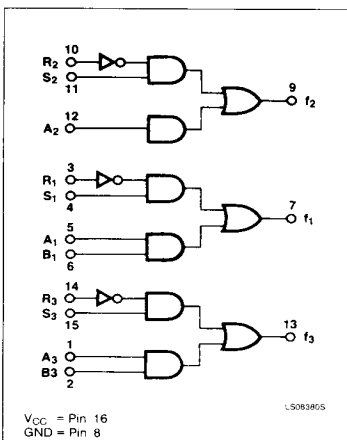
8T24 will also withstand an input of $-0.15V$ with power on or off.

The 8T24 is fully compatible with TTL and DTL systems and operates from a single 5 volt power supply.

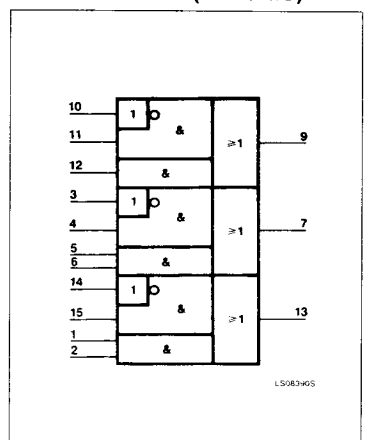
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Line Receiver

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ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		8T	UNIT
V _{CC}	Supply voltage	7.0	V
V _{IN}	Input voltage	-0.5 to +5.5	V
V _{OUT}	Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	V
T _A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		8T			UNIT
		Min	Nom	Max	
V _{CC}	Supply voltage	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage	2.0		2.5	V
V _{IL}	LOW-level input voltage	1.1		1.5	V
I _{IK}	Input clamp current			-12	mA
I _{OH}	HIGH-level output current			-800	μA
I _{OL}	LOW-level output current			16	mA
T _A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS ¹	8T24		UNIT
			Min	Max	
V _{IH}	Input HIGH voltage	Guaranteed input HIGH threshold voltage	1.7		V
V _{IL}	Input LOW voltage	Guaranteed input LOW threshold voltage		0.7	V
V _{IK}	Input clamp diode voltage	V _{CC} = MIN, I _{IK} = -12mA		-1.5	V
V _{OH}	HIGH-level output voltage	V _{CC} = MIN, I _{OH} = -800μA	2.6		V
V _{OL}	LOW-level output voltage	V _{CC} = MIN, I _{OL} = 16mA		0.4	V
I _{IH}	HIGH-level input current	V _{CC} = MAX, V _I = 4.5V, pins S, A, B		40	μA
		V _{CC} = MAX, V _I = 4.5V, pin R		170	μA
I _{IL}	LOW-level input current	V _{CC} = MAX, V _I = 0.4V		-1.6	mA
I _{OS}	Short-circuit output current ²	V _{CC} = MAX	-50	-100	mA
I _{CC}	Supply current (total)	V _{CC} = 5.25V		80	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

SWITCHING CHARACTERISTICS V_{CC} = 5.0V and T_A = 25°C

PARAMETER	TEST CONDITIONS				LIMITS			UNITS
	R	S	A	B	Min	Typ	Max	
t _{PHL}						20	30	ns
t _{PLH}						20	30	ns
Hysteresis ¹		4.5V	0V	0V	0.2	0.4		V

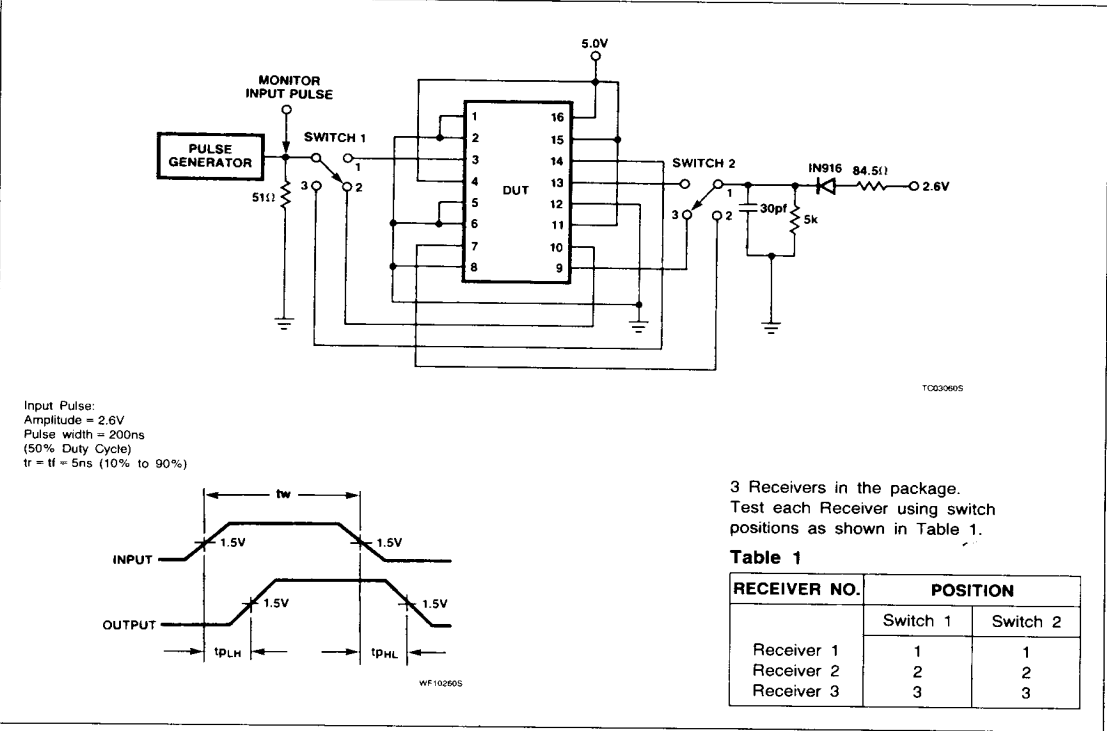
NOTE:

- Hysteresis is defined as the voltage difference between the R input level at which the output begins to go from "0" to "1" state and the level at which the output begins to go from "1" to "0".

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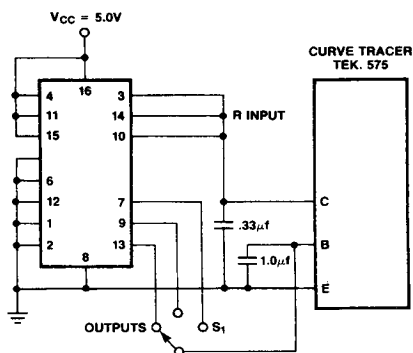
AC TEST CIRCUIT AND WAVEFORMS



Line Receiver

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HYSTERESIS TEST CIRCUIT



TC030705

Verify in each of three (3) position of S_1 (Figure 1) that the following occurs per Figure 2.

1. V_1 and V_2 must be between 0.7V minimum and 1.7 maximum.
2. Hysteresis = $V_1 - V_2$

